

Abstract of the Disclosure

Disclosed herein is a phase change memory provided with a write data register DIR, an output data selector DOS, a write address register AR, an address comparator ACP and a flag register FR. Write data is not only written into a memory cell but also retained by the write data register until the next write cycle. If a read access occurs to that address before the next write cycle, data is read out from the register without reading the data from the memory cell array.

Without elongating the cycle time, this makes it possible not only to use long time to write data into a memory cell therein but also to make longer the interval between the time when a write operation is done and the time when the subsequent read operation is made from that memory cell. As a result, data can be written reliably.